Basic Digital Logic Gates

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Contents

1 AIM

To verify the operation of basic logic gates NOT,AND,OR,NAND and NOR and also verify the operation of NOT,AND and OR by using the NAND and NOR only.

2 APPARATUS AND PARTS REQUIRED

Protoboard,DVM, Logic probe, 74LS00, 74LS02, 74LS08, 74LS32 ICs and connection wires.

3 THEORY

Digital systems are said to be constructed by using logic gates. These gates are the AND, OR, NOT, NAND, NOR, EXOR and EXNOR gates. The basic operations are described below with the aid of truth tables and IC diagram

3.1 NOT GATE

The NOT gate is an electronic circuit that produces an inverted version of the input at its output. It is also known as an inverter. If the input variable is A, the inverted output is known as NOT A. This is also shown as A', or A with a bar.

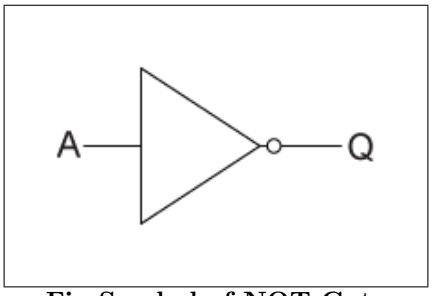


Fig Symbol of NOT Gate

A	$\overline{A}$
0	1
1	0

Fig Truth Table

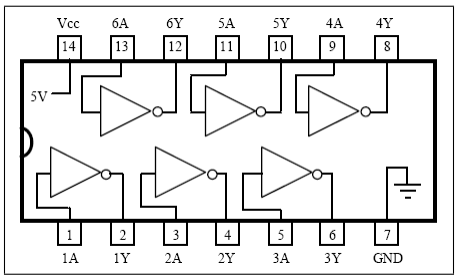


Fig IC Diagram

3.2 AND Gate

The AND gate is an electronic circuit that gives a high output (1) only if all its inputs are high. A dot (.) is used to show the AND operation i.e. A.B. Bear in mind that this dot is sometimes omitted i.e. AB

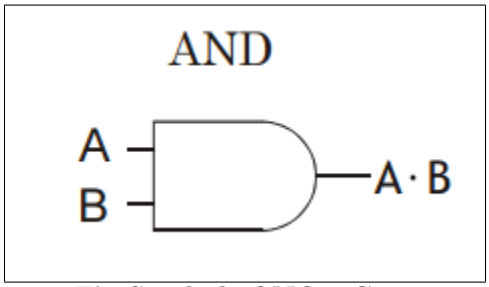


Fig Symbol of NOT Gate

A	B	A • B
0	0	0
0	1	0
1	0	0
1	1	1

Fig Truth Table

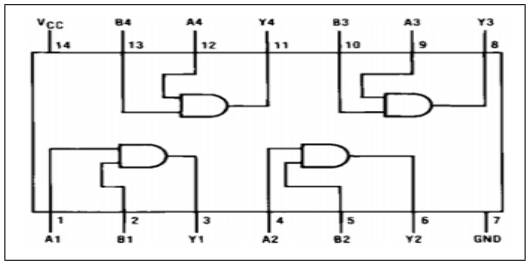


Fig IC Diagram

3.3 OR Gate

The OR gate is an electronic circuit that gives a high output (1) if one or more of its inputs are high. A plus (+) is used to show the OR operation.

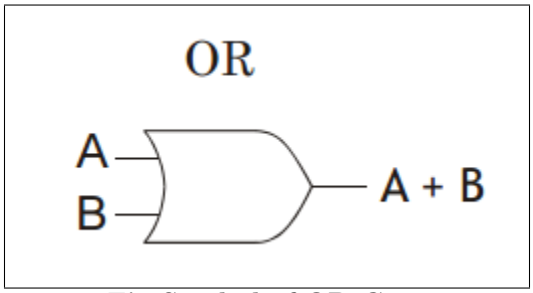


Fig Symbol of OR Gate

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

Fig Truth Table

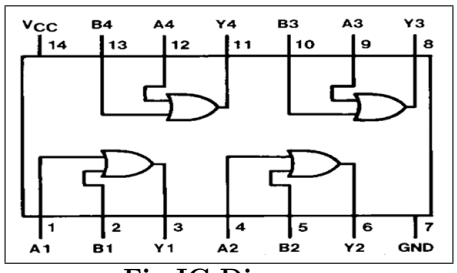


Fig IC Diagram

3.4 NAND Gate

This is a NOT-AND gate which is equal to an AND gate followed by a NOT gate. The outputs of all NAND gates are high if any of the inputs are low. The symbol is an AND gate with a small circle on the output. The small circle represents inversion.

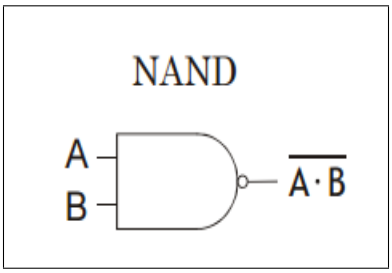


Fig Symbol of NAND Gate

A	B	$\overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

Fig Truth Table

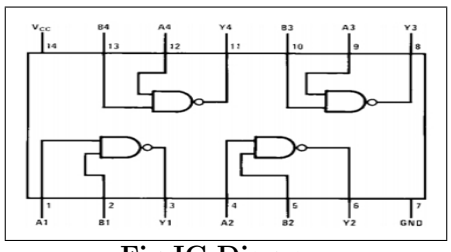


Fig IC Diagram

3.5 NOR Gate

This is a NOT-OR gate which is equal to an OR gate followed by a NOT gate. The outputs of all NOR gates are low if any of the inputs are high.The symbol is an OR gate with a small circle on the output. The small circle represents inversion.

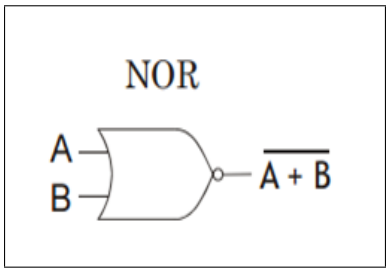


Fig Symbol of NOR Gate

A	B	$\overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

Fig Truth Table

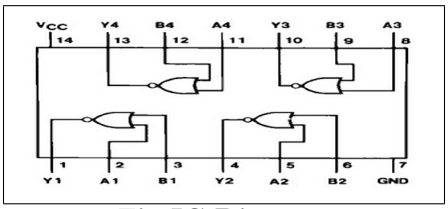
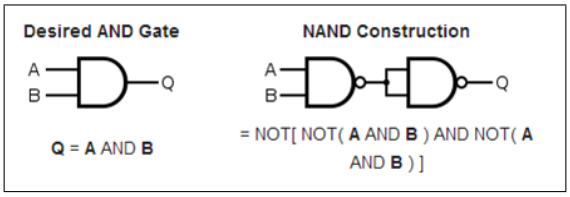


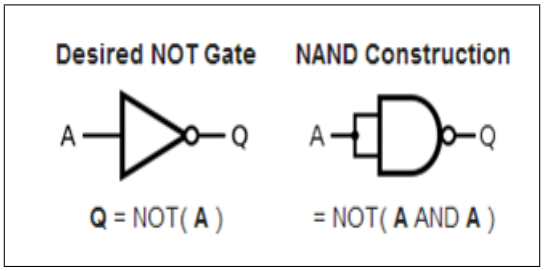
Fig IC Diagram

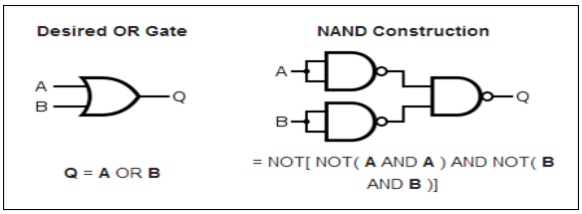
3.6 AND,NOT and OR gates using Universal Gates

NAND and NOR gates are universal gates because we can implement all the gates from these gates .There are the figures of gates that is implemented by NAND and NOR gates

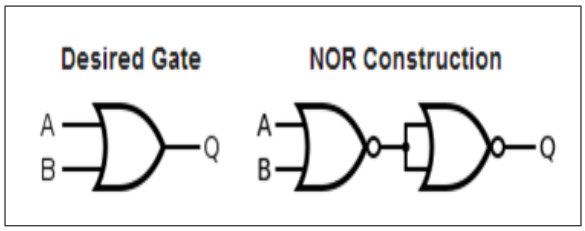
Using NAND

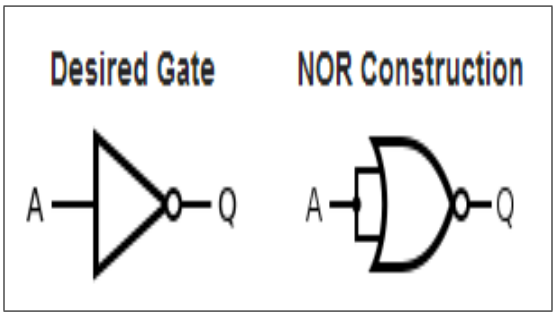


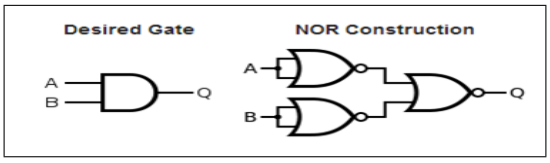




Using NOR







4 OBSERVATION TABLES

Table 1: AND GATE

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.125
2	0	1	low	0.135
3	1	0	low	0.110
4	1	1	high	4.82

Table 2: NOT GATE

Sl No.	Input	Output	
	A	Q	Voltage(in V)
1	0	low	0.06
2	1	high	3.06

Table 3: OR GATE

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.021
2	0	1	high	3.222
3	1	0	high	3.82
4	1	1	high	4.64

Table 4: NAND GATE

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	high	5.01
2	0	1	high	5.0
3	1	0	high	5.0
4	1	1	low	0.001

Table 5: NOR GATE

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	high	4.65
2	0	1	low	0.737
3	1	0	low	0.131
4	1	1	low	0.107

Table 6: AND GATE USING NAND

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.027
2	0	1	low	0.049
3	1	0	low	0.037
4	1	1	high	5

Table 7: NOT GATE USING NAND

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	1	1	low	0.007
2	0	0	high	5

Table 8: OR GATE USING NAND

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.014
2	0	1	high	3.25
3	1	0	high	3.45
4	1	1	high	3.64

Table 9: AND GATE USING NOR

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.104
2	0	1	low	0.153
3	1	0	low	0.275
4	1	1	high	3.82

Table 10: NOT GATE USING NOR

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	1	1	low	0.06
2	0	0	high	3.06

Table 11: OR USING NOR

Sl No.	Input		Output	
	A	B	Q	Voltage(in V)
1	0	0	low	0.02
2	0	1	high	3.82
3	1	0	high	3.92
4	1	1	high	3.84

5 RESULTS

All the gates and their truth tables verified successfully and we also implemented and verified gates using universal gates .

6 PRECAUTIONS

1.Make the connections using IC pin diagram
2.The connections should be tight.
3.The Vcc and Ground should be connect carefully at the specified pin only
4.Take all the readings carefully and sharply by the multimeter.

7 REFERENCES

1.www.wikipedia.com
2.Lab manual
3.Digital Logic Book by Morris Mano